

IN610

Bluetooth 5 Wireless SoC



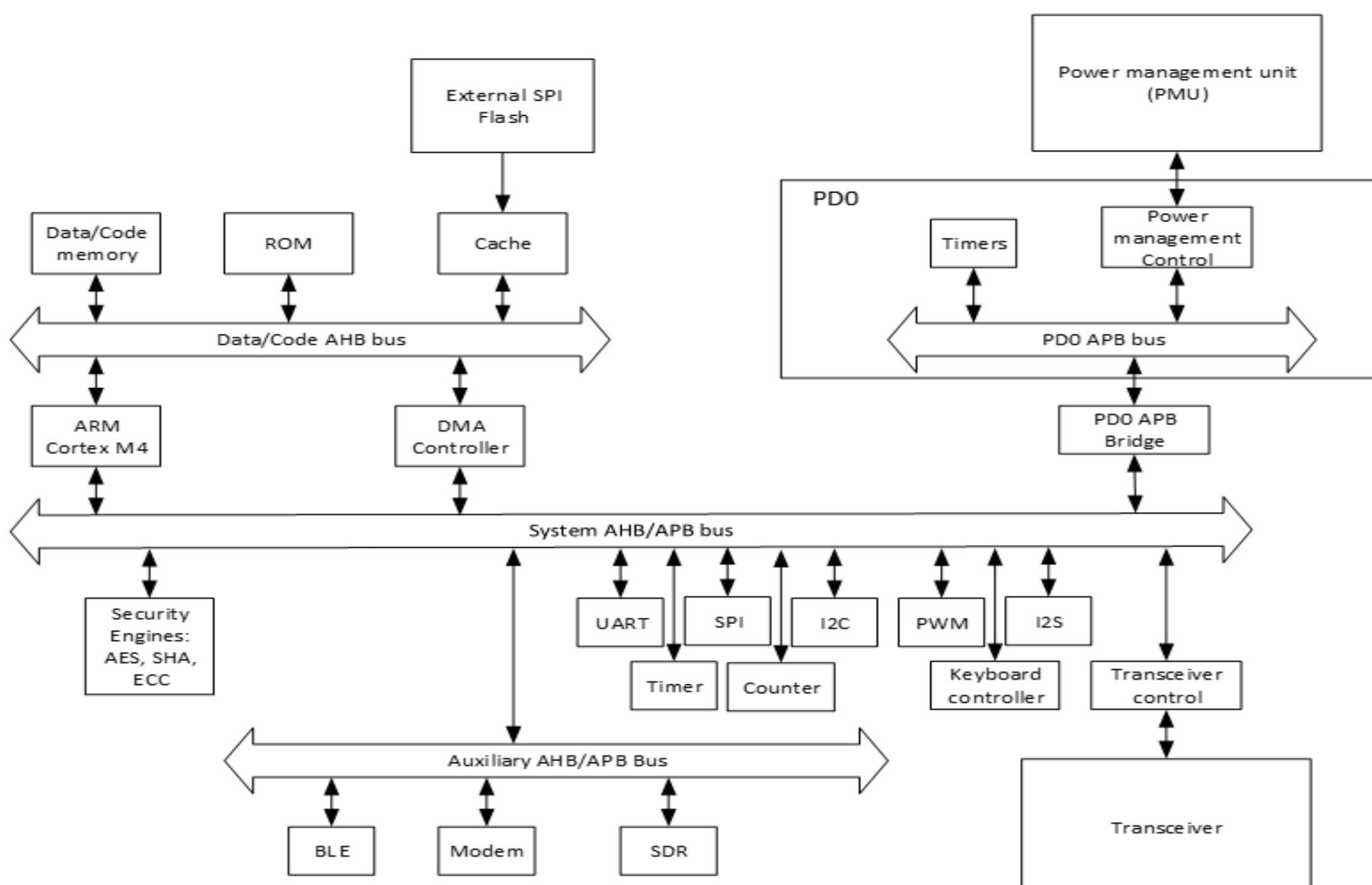
- High data rate supports up to 2Mbps
- The world's leading RF performance
- Ultra low power consumption
- High security

N610 integrates a powerful 32bit ARM Cortex-M4F CPU with floating point unit processing capability. It has built-in 256KB ROM, up to 1MB Flash memory and high density up to 96KB SRAM which can be used as user data space for sophisticated algorithms and applications.

The device has an excellent RF performance with ultra-low power consumption design philosophy in mind, so it is well suited for power constraint applications such as battery powered products (ex. retail beacon and wearables). Along with the powerful ARM Cortex-M4F CPU and rich memory resources integrated into the device, user can develop as many applications without adding additional CPU.

The device has well-crafted hardware security engine designed which supports AES128, AES256, SHA-1, SHA-2 and ECC encryption and decryption algorithms. It also has True Random Number Generator (TRNG) integrated to facilitate security application implementation. The security engine includes two independent sets of crypto engines which to serve not only the Bluetooth 5 radio link layer enhanced security but also user application security requirement.

In addition to the sophisticated design on radio and communication modems, the device integrates variety of peripherals such as I2C, SPI, UART, PDM and I2S for user applications. IN610 comes with package option of QFN48.



IN610 Features

Protocol Stack

- Bluetooth 5 compliant
- High data rate supports up to 2Mbps

CPU & Memory

- ARM Cortex-M4F up to 64MHz with 16KB i-cache
- 256KB ROM (bootloader & SW stack)
- Up to 96KB user SRAM
- 4Kb eFuse memory (Manufacturer ID, Security Key storage)
- 512KB Flash memory (Stacked, XIP mode support)
- Over-The-Air Update (OTA) support
- SWD/JTAG debug interface

Radio

- 2.4GHz transceiver, Bluetooth 5 compliant
- Rx sensitivity -104.5 dBm @ 125Kbps
- Rx sensitivity -97.5 dBm @ 1Mbps
- Rx sensitivity -94.5 dBm @ 2Mbps
- Tx output 0dBm, 4.1mA, up to +3 dBm
- Rx 5mA
- Link budget of 107.5 dB @ 125Kbps

Power mode

- Deep Sleep mode 500nA with 32KHz RC ON
- Shutdown mode <20nA

Clock Source

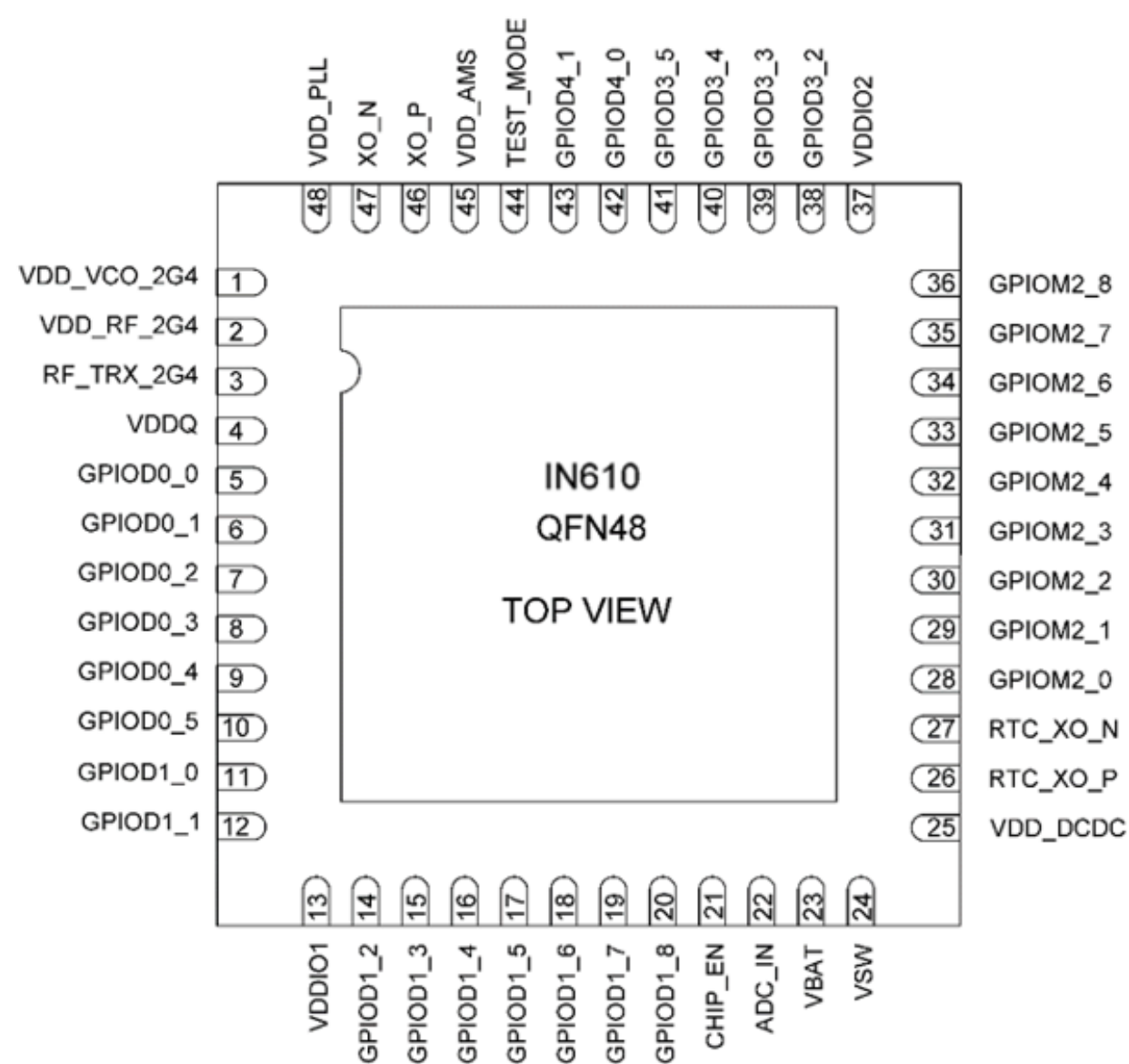
- 32MHz crystal, 32.768KHz RTC

Peripheral Interface

- Up to 30 GPIOs
- 2 I2C, master/slave up to 400KHz clock
- 1 SPI master w/ up to 4 SPI slaves supported, up to 16MHz clock
- 1 SPI slave, up to 4MHz clock
- 2 UART up to 2MHz
- 5 dedicated PWMs, up to 13 PWM through I/O configuration
- 1 I2S master and 1 I2S slave, bi-directional stereo support
- 2 PDM mono or 1 stereo with clock range from 160KHz - 5.12MHz
- ISO7816
- Keyboard scanner - up to 14x14 matrix
- QDEC
- 11-bit ADC, up to 1MSPS, up to 10 channels
- 8 counters/timers

Security

- HW ECC, AES256, SHA-1, SHA-2
- Secure Boot, Software copyright protection



Pin No.	Pin Name	JLINK	UART	I2C	SPI	I2S	PWM COUNTER	PDM
5	GPIO_0_0		UART0_RTS	I2C0_SCL			PWM0	
6	GPIO_0_1		UART0_CTS	I2C0_SDA	SPI_MST_MISO_BKU		PWM1	
7	GPIO_0_2		UART0_TX				PWM2	
8	GPIO_0_3			I2C1_SCL	SPI_MST_MOSI_BKU			
9	GPIO_0_4			I2C1_SDA	SPI_MST_CLK_BKU			
10	GPIO_0_5							
11	GPIO_1_0		UART0_RX					
12	GPIO_1_1	TMS/SWDIO						
14	GPIO_1_2	TCK/SCK						
15	GPIO_1_3	TDO				I2S_MST/SLV_CLK		
16	GPIO_1_4	TDI				I2S_MST/SLV_WS		
17	GPIO_1_5		UART1_RTS			I2S_MST/SLV_SD0		
18	GPIO_1_6		UART1_CTS			I2S_MST_SD1/SLV_SD0		
19	GPIO_1_7		UART1_TX	I2C0_SCL_BKU			PWM3	
20	GPIO_1_8		UART1_RX	I2C0_SDA_BKU			PWM4	
28	GPIO_2_0							
29	GPIO_2_1		UART1_TX_BKU		SPI_MST_SSN1		COUNTER0	
30	GPIO_2_2						COUNTER1	
31	GPIO_2_3		UART0_TX_BKU				COUNTER2	
32	GPIO_2_4						COUNTER3	
33	GPIO_2_5		UART0_RX_BKU				COUNTER4	
34	GPIO_2_6						COUNTER5	
35	GPIO_2_7		UART1_RX_BKU				COUNTER6	PDM1_DAT
36	GPIO_2_8						COUNTER7	PDM0_DAT
38	GPIO_3_2				SPI_MST_SSN2			
39	GPIO_3_3				SPI_MST_SSN3			
40	GPIO_3_4				SPI_MST/SLV_CLK			
41	GPIO_3_5				SPI_MST/SLV_MISO			PDM_CLK
42	GPIO_4_0			I2C1_SCL_BKU	SPI_MST/SLV_MOSI			
43	GPIO_4_1			I2C1_SDA_BKU	SPI_MST/SLV_SSN0			