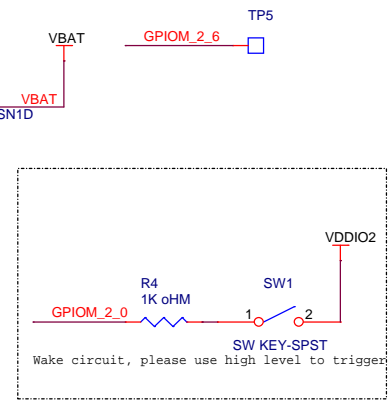
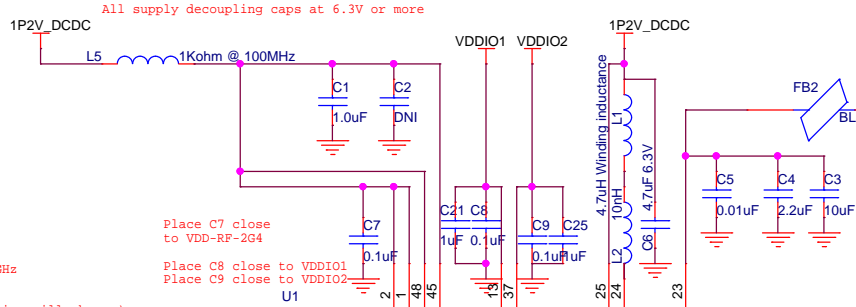


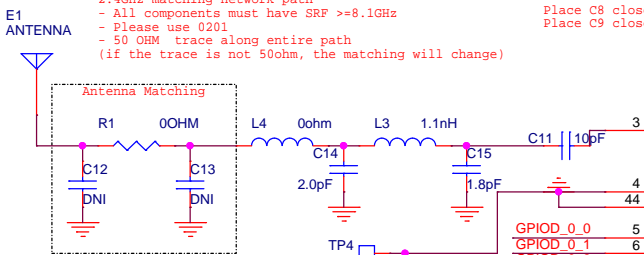
## Power Input



Re-Programming pin,  
Connect to low : reprogram,  
Floating or High: run bootram into application

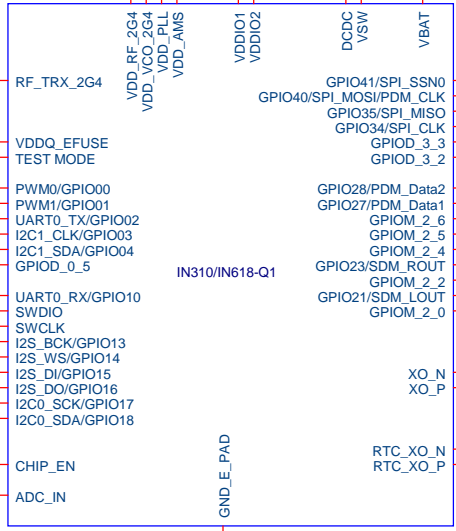


2.4GHz matching network path  
- All components must have SRF >=8.1GHz  
- Please use 0201  
- 50 OHM trace along entire path  
(if the trace is not 50ohm, the matching will change)

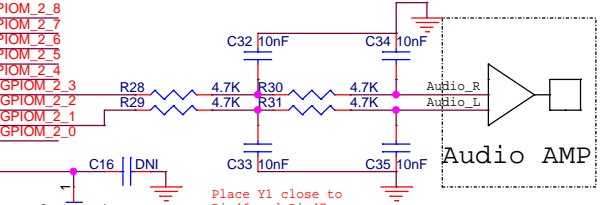


VDDQ connect 3.3V when efuse programming

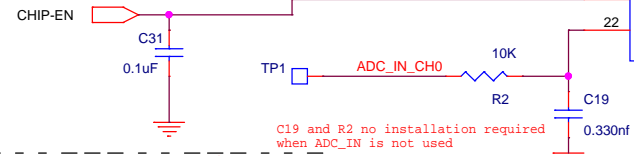
Test Point or Header for access to debug pins



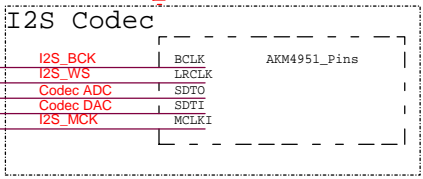
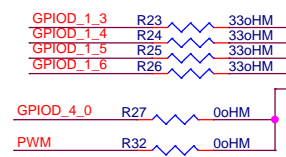
## SDM Output with RC filter



Chip\_en Can be connected to VBAT directly through a series 1K resistor



Debug Interface: Jlink  
Programming Port: Jlink & Uart  
Print LOG: UART  
Efuse enable pin: VDDQ to 3.3V  
Program Pin: GPIO26



For detail GPIO pinmux,  
Please find in datasheet

PWM Clock range is an integral multiple of 32M  
GPIO00, GPIO01, GPIO02, GPIO17, GPIO18 can used for PWM

For different Codec, Please select the correct MCLK clock source.  
It is prefer to use external crystal.

Title		
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