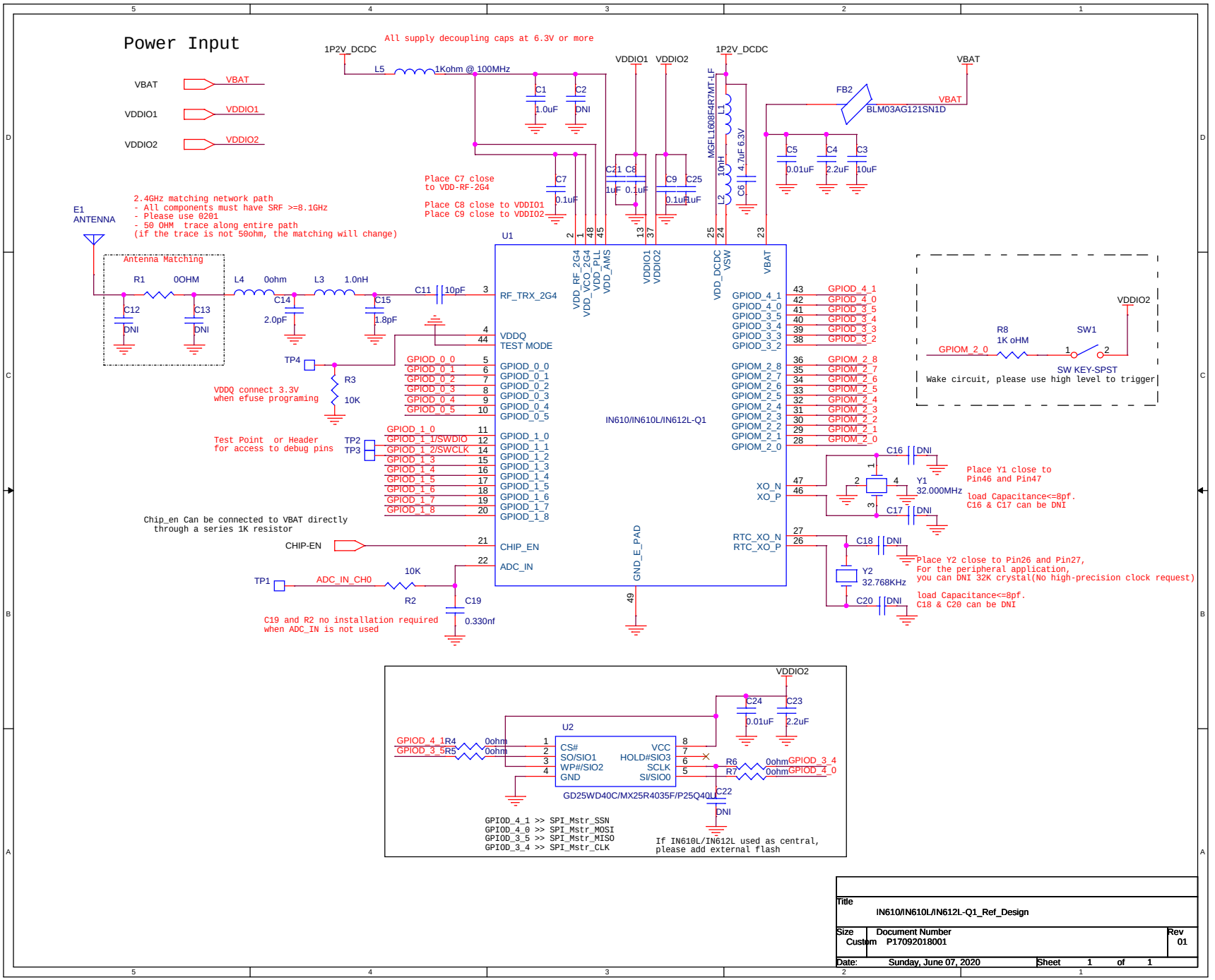
Power Input
All supply decoupling caps at 6.3V or more
1P2V_DCDC
L5
1Kohm @ 100MHz
C1
1.0uF
C2
DNI
VDDIO1
VDDIO2
VBAT
FB2
BLM03AG121SN1D
MGFL1608F4R7MT-LF
L1
10nH
L2
C6
4.7uF 6.3V
C5
0.01uF
C4
2.2uF
C3
10uF
C7
0.1uF
C21
1uF
C8
0.1uF
C9
0.1uF
C25
1uF
Place C7 close to VDD-RF-2G4
Place C8 close to VDDIO1
Place C9 close to VDDIO2
E1
ANTENNA
2.4GHz matching network path
- All components must have SRF >=8.1GHz
- Please use 0201
- 50 OHM trace along entire path
(if the trace is not 50ohm, the matching will change)
Antenna Matching
R1
0OHM
L4
0ohm
L3
1.0nH
C12
DNI
C13
DNI
C14
2.0pF
C15
1.8pF
C11
10pF
U1
RF_TRX_2G4
VDDQ
TEST MODE
IN610/IN610L/IN612L-Q1
GND_E_PAD
VDD_RF_2G4
VDD_VCO_2G4
VDD_PLL
VDD_AMS
VDD_DCDC
VSW
GPIOD_0_0
GPIOD_0_1
GPIOD_0_2
GPIOD_0_3
GPIOD_0_4
GPIOD_0_5
GPIOD_1_0
GPIOD_1_1/SWDIO
GPIOD_1_2/SWCLK
GPIOD_1_3
GPIOD_1_4
GPIOD_1_5
GPIOD_1_6
GPIOD_1_7
GPIOD_1_8
GPIOM_2_8
GPIOM_2_7
GPIOM_2_6
GPIOM_2_5
GPIOM_2_4
GPIOM_2_3
GPIOM_2_2
GPIOM_2_1
GPIOM_2_0
TP4
R3
10K
VDDQ connect 3.3V
when efuse programing
TP2
TP3
Test Point or Header
for access to debug pins
Chip_en Can be connected to VBAT directly
through a series 1K resistor
CHIP-EN
CHIP_EN
ADC_IN
TP1
ADC_IN_CH0
10K
R2
C19
0.330nf
C19 and R2 no installation required
when ADC_IN is not used
XO_N
XO_P
C16
DNI
Y1
32.000MHz
C17
DNI
Place Y1 close to
Pin46 and Pin47
load Capacitance<=8pf.
C16 & C17 can be DNI
RTC_XO_N
RTC_XO_P
C18
DNI
Y2
32.768KHz
C20
DNI
Place Y2 close to Pin26 and Pin27,
For the peripheral application,
you can DNI 32K crystal(No high-precision clock request)
load Capacitance<=8pf.
C18 & C20 can be DNI
R8
1K oHM
SW1
SW KEY-SPST
Wake circuit, please use high level to trigger
U2
GD25WD40C/MX25R4035F/P25Q40L
GPIOD_4_1R4
GPIOD_3_5R5
0ohm
CS#
SO/SIO1
WP#/SIO2
GND
VCC
HOLD#SIO3
SCLK
SI/SIO0
R6
R7
C22
DNI
C24
0.01uF
C23
2.2uF
GPIOD_4_1 >> SPI_Mstr_SSN
GPIOD_4_0 >> SPI_Mstr_MOSI
GPIOD_3_5 >> SPI_Mstr_MISO
GPIOD_3_4 >> SPI_Mstr_CLK
If IN610L/IN612L used as central,
please add external flash
Title
IN610/IN610L/IN612L-Q1_Ref_Design
Size
Custom
Document Number
P17092018001
Rev
01
Date:
Sunday, June 07, 2020
Sheet
1
of
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